REMARKS

Claims 1, 3, and 6 are amended. No new subject matter is added. Reconsideration and allowance of claims 1-7 is requested in light of the following remarks.

Claim Rejections – 35 USC § 102

Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,856,918 to Soneda et al. ("Soneda"). The applicants disagree.

Claim 1 is amended for improved clarity. No new subject matter is added. Claim 3 is amended to depend from claim 2 rather than claim 1. No new subject matter is added.

It is generally alleged that Soneda FIG. 2 shows a circuit with elements that operate "similarly" as recited in claim 1. However, "similarly" is not the standard that should be applied to 35 U.S.C. § 102 rejections. A claim is anticipated only if the reference shows the ***identical*** invention in as complete detail as contained in the claim. MPEP 2131, *citing* Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236 (Fed. Cir. 1989), emphasis added.

Claim 1 recites boosting capacitors that include a first and a last boosting capacitor, the first boosting capacitor connected to a driving node and the last boosting capacitor configured to output a boosting voltage. Claim 1 also recites that a voltage level at the driving node changes according to a logic state of a boosting level control signal.

It is specifically alleged that Soneda FIG. 2 teaches boosting capacitors C1-C3 (FIG. 2). Thus, Soneda's capacitor C1 is apparently considered the recited first boosting capacitor, and Soneda's capacitor C3 is apparently considered the recited last boosting capacitor. Furthermore, Soneda's circuit node K1 (FIG. 2; input to capacitor C1) is apparently considered the recited driving node and Soneda's circuit node L3 (FIG. 2; output of capacitor C3) is apparently considered the boosting voltage.

It has not been alleged which signals shown in Soneda FIG. 2 are the recited control signal and the recited boosting level control signal. It is evident that only the signals CLK1, CLK2, and CLK3 (FIG. 2) could be the recited control signal and the recited boosting level control signal because the reference voltage GND (FIG. 2) and the supply voltage V_{CC} (FIG. 2) are generally understood to be constant.

Claim 1 recites that the switches are configured to connect the boosting capacitors in series in response to a control signal. Thus, Soneda's CLK3 signal is apparently considered the recited control signal as this signal controls the switching means PT1, PT2, PT3 (FIG. 2).

Therefore, only the remaining signals CLK1 and CLK2 are candidates for the recited boosting level control signal. However, contrary to the recited features of claim 1, it is clearly illustrated that a voltage level at the alleged driving node K1 (FIG. 4D) does not have a logic state that changes according to a logic state of the signal CLK1 (FIG. 4A) or the signal CLK2 (FIG. 4C). Thus, neither of the signals CLK1 or CLK2 can be the recited boosting level control signal.

Consequently, Soneda fails to anticipate claim 1 because it does not show the identical invention in as complete detail as contained in the claim. MPEP 2131.

Claims 2-5 depend from claim 1, and inherently contains the features of claim 1. Consequently, Soneda fails to anticipate claims 2-5 for the same reason discussed above for claim 1. MPEP 2131.

Furthermore, claim 2 recites that when the boosting level control signal is in a first logic state, the voltage level at the driving node changes from a ground voltage level to an external supply voltage level.

Contrary the above feature of claim 2, it is apparent that the voltage level at the alleged driving node K1 (FIG. 4D) does not change from a ground voltage level to an external supply voltage level when the boosting level control signal [either CLK1 (FIG. 4A) or CLK2 (FIG. 4C)] is in a first logic state.

Consequently, Soneda fails to anticipate claim 2 for the additional reason discussed above. MPEP 2131.

Claim 3 depends from claim 2, and inherently contains the features of claim 2. Consequently, Soneda fails to anticipate claim 3 for the same reason discussed above for claim 2. MPEP 2131.

Furthermore, claim 4 recites that the logic state of the boosting level control signal is configured to enter a logic high state or a logic low state in response to an external supply voltage level.

Contrary to the above feature of claim 4, there is no indication that Soneda's signals CLK1 (FIG. 4A) or CLK2 (FIG. 4C) are configured to enter a logic high state or a logic low state in response to the external supply voltage V_{CC}. See, e.g., FIG. 2, where the signals CLK1 and CLK2 are independent of the external supply voltage VCC.

Consequently, Soneda fails to anticipate claim 4 for the additional reason discussed above. MPEP 2131.

Claim 5 recites that the external supply voltage detector is configured to detect the external supply voltage level and to generate the boosting level control signal.

Contrary to the above feature of claim 5, there is no indication in Soneda FIG. 2 that the alleged external supply voltage detectors (NU1, NU2, or NU3) are configured to generate the alleged boosting level control signal (either CLK1 or CLK2).

Consequently, Soneda fails to anticipate claim 5 for the additional reason discussed above. MPEP 2131.

Claim 6 is amended both for improved clarity and to recite a feature that is found in the specification. The amendments to claim 6 are fully supported by the original application at, e.g., claim 6 and page 5, lines 4-6. Thus, no new subject matter is added.

Claim 6 recites, *inter alia*, decreasing the boosting voltage by an amount approximately equal to the external supply voltage level by fixing the voltage level at the driving node to the ground voltage level when the boosting level control signal is in a second logic state.

As was explained above in the discussion regarding claim 1, Soneda's node K1 (FIG. 2) is apparently alleged to be the recited driving node, Soneda's node L3 (FIG. 2) is apparently alleged to be the recited boosting voltage, and either Soneda's signal CLK1 or CLK2 (FIG. 2) is alleged to be the recited boosting level control signal.

Contrary to claim 6, it can be seen in FIG. 4I that the alleged boosting voltage L3 is not decreased by an amount approximately equal to the external supply voltage by fixing the voltage level at the alleged driving node K1 (FIG. 4D) to the ground voltage level. Rather, the alleged boosting voltage L3 is decreased from a level that is approximately $4V_{CC}$ to a level that is less than $2V_{CC}$ (FIG. 4I). In other words, the amount by which the alleged boosting voltage L3 is decreased is greater than $2V_{CC}$.

Consequently, Soneda fails to anticipate claim 6 because it does not show the identical invention in as complete detail as contained in the claim. MPEP 2131.

Claim 7 depends from claim 6 and inherently contains the features of claim 6. Consequently, Soneda fails to anticipate claim 7 for the same reason discussed above for claim 6. MPEP 2131.

Furthermore, claim 7 recites changing the boosting level control signal to the first logic state when the external supply voltage level is less than a reference voltage level, and changing the boosting level control signal to the second logic state when the external supply voltage level is greater than the reference voltage level.

Contrary to the above features of claim 7, Soneda does not teach that the alleged boosting level control signal [either CLK1 (FIG. 4A) or CLK2 (FIG. 4C)] is changed to a first logic state when the external supply voltage level V_{CC} is less than a reference voltage

level, nor does it teach that the alleged boosting level control signal CLK1 or CLK2 is changed to the second logic state when the external supply voltage V_{CC} is greater than the reference voltage level.

Consequently, Soneda fails to anticipate claim 7 for the additional reason discussed above. MPEP 2131.

Conclusion

For the above reasons, reconsideration and allowance of claims 1-7 is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.

Todd J. Iverson
Reg. No. 53,057

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613
Customer No. 20575

I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (703) 872-9306 on March 29, 2005.

Li Mei Vermilya